We claim:

1. A pre-drive circuit comprising: a plurality of drive systems each having an input amplifier circuit for amplifying an input voltage input to an input voltage terminal; a high level shift circuit for shifting a level of a signal output from the input amplifier circuit; and an output amplifier circuit for amplifying a shift signal output from the high level shift circuit, wherein each drive system has the same constitution.

2. A pre-drive circuit as set forth in claim 1, wherein a power supply terminal for supplying the drive power supply of the input amplifier circuit of the plurality of drive systems and a power supply terminal for supplying the drive power supply of the output amplifier circuit of the plurality of drive systems are provided separately.

3. A pre-drive circuit as set forth in claim 2, further comprising waveform processing circuits each of which is provided between the input voltage terminal and the input amplifier circuit of each of the drive systems.

4. A pre-drive circuit as set forth in claim 3, further comprising a power supply terminal for the waveform processing circuit.

5. A pre-drive circuit as set forth in claim 3, further comprising a constant voltage circuit that generates a supply voltage for the waveform processing circuit by converting a voltage to be supplied to the power supply terminal for the input amplifier circuit and supplies the generated voltage as a supply voltage to the waveform processing circuit.

6. A pre-drive circuit as set forth in claim 1, wherein each drive system includes a low level shift circuit for shifting a level of a signal output from the input amplifier circuit to a signal referred to a negative reference voltage, and the high level shift circuit shifts the level of the signal output from the low level shift circuit.

7. A pre-drive circuit as set forth in claim 6, wherein each drive system includes a waveform processing circuit for processing a waveform of the signal output from the low level shift circuit, the high level shift circuit shifts the level of the signal output from the waveform processing circuit, and the waveform processing circuit is connected to a negative reference voltage input terminal, to which the negative voltage is input, and a negative supply voltage input terminal, to which a negative supply voltage having a predetermined voltage referred to the negative reference voltage.

8. A pre-drive circuit as set forth in claim 7, wherein a power supply terminal for supplying a drive power supply of the input amplifier circuits of the plurality of drive systems, and a power supply terminal for supplying a drive power supply of the output amplifier circuits of the plurality of drive systems and the negative supply voltage input terminal, are separately provided.

9. A pre-drive circuit as set forth in claim 3, wherein the waveform processing circuit is a Schmitt trigger circuit.

10. A pre-drive circuit as set forth in claim 7, wherein the waveform processing circuit is a Schmitt trigger circuit.

11. A pre-drive circuit as set forth in claim 7, the waveform processing circuit has an integrating circuit for eliminating noise.

12. A pre-drive circuit as set forth in claim 1, wherein a threshold voltage of the input amplifier circuit is an intermediate between potentials of the supply voltage of the input amplifier circuit.

13. A pre-drive circuit as set forth in claim 1, wherein the plurality of drive systems are provided within one package.

14. A pre-drive circuit as set forth in claim 1, wherein the plurality of drive systems are provided

within an IC formed on the same semiconductor chip.

15. A pre-drive circuit as set forth in claim 1, wherein the pre-drive circuit includes two of the drive systems.

16. A pre-drive circuit as set forth in claim 1, wherein the pre-drive circuit includes four of the drive systems.

17. A pre-drive circuit as set forth in claim 6, wherein the pre-drive circuit includes two of the drive systems.

18. A pre-drive circuit as set forth in claim 6, wherein the pre-drive circuit includes four of the drive systems.

19. A pre-drive circuit as set forth in claim 17, wherein two of the drive systems of the plurality of drive systems are paired, and each pair includes a simultaneous ON avoiding circuit for maintaining an output of one of the two drive systems of the pair to be inactive when an output of the other of the two drive systems of the pair is active.

20. A capacitive load drive circuit comprising: the pre-drive circuit set forth in claim 15; a first switch element connected to an output of the output amplifier circuit of one of the plurality of drive systems of the pre-drive circuit; and a second switch element connected to an output of the output amplifier circuit of the other of the plurality of drive systems, wherein a high level voltage is supplied to a capacitive load via the first switch element and a low level voltage is supplied to the capacitive load via the second switch element.

21. A capacitive load drive circuit comprising: first and second pre-drive circuits each of which is the pre-drive circuit set forth in claim 15; a first switch element connected to an output of the output amplifier circuit of one of the plurality of drive systems of the first pre-drive circuit; a second switch element connected to an output of the output amplifier circuit of

the other of the plurality of drive systems of the first pre-drive circuit; a third switch element connected to an output of the output amplifier circuit of one of the plurality of drive systems of the second pre-drive circuit; and a fourth switch element connected to an output of the output amplifier circuit of the other of the plurality of drive systems of the second pre-drive circuit, wherein a high level voltage is supplied to a capacitive load via the first switch element, a low level voltage is supplied to the capacitive via the second switch element, the high level voltage is supplied to the capacitive load via the third switch element and a first coil connected in series to the third switch element, and the low level voltage is supplied to the capacitive load via the fourth switch and a second coil connected in series to the fourth switch element.

22. A capacitive load drive circuit comprising: a pre-drive circuit as set forth in claim 16; a first switch element connected to an output of the output amplifier circuit of a first drive system of the plurality of drive systems of the pre-drive circuit; a second switch element connected to an output of the output amplifier circuit of a second drive system of the plurality of drive systems of the pre-drive circuit; a third switch element connected to an output of the output amplifier circuit of a third drive system of the plurality of drive systems of the pre-drive circuit; and a fourth switch element connected to an output of the output amplifier circuit of a fourth drive system of the plurality of drive systems of the pre-drive circuit, wherein a high level voltage is supplied to a capacitive load via the first switch element, a low level voltage is supplied to the capacitive via the second switch element, the high level voltage is supplied to the capacitive load via the third switch element and a first coil connected in series to the third switch element, and the low level voltage is supplied to the capacitive load via the fourth

switch and a second coil connected in series to the fourth switch element.

23. A capacitive load drive circuit comprising: the pre-drive circuit set forth in claim 17; a first switch element connected to an output of the output amplifier circuit of one of the plurality of drive systems of the pre-drive circuit; and a second switch element connected to an output of the output amplifier circuit of the other of the plurality of drive systems, wherein a high level voltage is supplied to a capacitive load via the first switch element and a low level voltage is supplied to the capacitive load via the second switch element.

24. A capacitive load drive circuit comprising: first and second pre-drive circuits each of which is the pre-drive circuit set forth in claim 17; a first switch element connected to an output of the output amplifier circuit of one of the plurality of drive systems of the first pre-drive circuit; a second switch element connected to an output of the output amplifier circuit of the other of the plurality of drive systems of the first pre-drive circuit; a third switch element connected to an output of the output amplifier circuit of one of the plurality of drive systems of the second pre-drive circuit; and a fourth switch element connected to an output of the output amplifier circuit of the other of the plurality of drive systems of the second pre-drive circuit, wherein a high level voltage is supplied to a capacitive load via the first switch element, a low level voltage is supplied to the capacitive via the second switch element, the high level voltage is supplied to the capacitive load via the third switch element and a first coil connected in series to the third switch element, and the low level voltage is supplied to the capacitive load via the fourth switch and a second coil connected in series to the fourth switch element.

25. A capacitive load drive circuit comprising: a pre-drive circuit set forth in claim 18; a first switch

element connected to an output of the output amplifier circuit of a first drive system of the plurality of drive systems of the pre-drive circuit; a second switch element connected to an output of the output amplifier circuit of a second drive system of the plurality of drive systems of the pre-drive circuit; a third switch element connected to an output of the output amplifier circuit of a third drive system of the plurality of drive systems of the pre-drive circuit; and a fourth switch element connected to an output of the output amplifier circuit of a fourth drive system of the plurality of drive systems of the pre-drive circuit, wherein a high level voltage is supplied to a capacitive load via the first switch element, a low level voltage is supplied to the capacitive via the second switch element, the high level voltage is supplied to the capacitive load via the third switch element and a first coil connected in series to the third switch element, and the low level voltage is supplied to the capacitive load via the fourth switch and a second coil connected in series to the fourth switch element.

26. A capacitive load drive circuit as set forth in claim 20, wherein the previous stage or the subsequent stage of the pre-drive circuit comprises a delay time adjusting circuit for adjusting an input and output time of a signal.

27. A capacitive load drive circuit as set forth in claim 20, wherein a voltage different from the reference voltage is applied to a terminal of the third switch element other than the terminal to be connected to the capacitive load.

28. A capacitive load drive circuit as set forth in claim 20, wherein a voltage other than the middle voltage of the high level voltage and the low level voltage is supplied to a terminal of the third switch element other than the terminal to be connected to the capacitive load.

29. A capacitive load drive circuit as set forth in

claim 20, wherein the high level voltage is the supply voltage and the low level voltage is the ground voltage.

30. A capacitive load drive circuit as set forth in claim 20, wherein the high level voltage is a positive voltage and the low level voltage is a negative voltage the absolute value of which is the same as that of the high level voltage.

31. A capacitive load drive circuit as set forth in claim 20, wherein the previous stage of the plurality of input voltage terminals of the pre-drive circuit comprises an input level shift circuit for converting in level an input signal referred to the ground voltage into one referred to the low level voltage.

32. A capacitive load drive circuit as set forth in claim 23, wherein the negative reference voltage is same as a low level voltage supplied to the second output element.

33. A capacitive load drive circuit as set forth in claim 23, wherein the negative reference voltage is different from a low level voltage supplied to the second output element.

34. A plasma display apparatus comprising: a plurality of X electrodes; a plurality of Y electrodes arranged adjacently to the plurality of X electrodes by turns and each causing a discharge to occur between the neighboring X and Y electrodes; an X electrode drive circuit for applying a discharge voltage to the plurality of X electrodes; and a Y electrode drive circuit for applying a discharge voltage to the plurality of Y electrodes, wherein at least one of the X electrode drive circuit and the Y electrode drive circuit is the capacitive load drive circuit set forth in claim 20.

35. A plasma display apparatus as set forth in claim 34, wherein a reset pulse is supplied to at least one of the X and Y electrodes, and the capacitive load drive circuit increases a low voltage, which is applied to the second terminal of the second output element, when

the reset pulse is supplied.